VARIABLE GAIN POWER AMPLIFIER FOR MOBILE WCDMA APPLICATIONS

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***Abstract* — A single chip linear power amplifier (PA) with > 48 dB gain control range and > 24 dBm output power with adjacent channel leakage power (ACP) figures below -36 dBc is presented. The chip is realized using an AlGaAs/GaAs HBT process and is aimed for 1.95 GHz mobile WCDMA applications. The amplifier consists of two blocks, the variable gain amplifier and the power amplifier. The chip size is 1.3x1.1 mm^2 and it is mounted on a 8x8 mm^2 FR-4 type laminate with 26 pieces of 0402 SMD components composing a complete 50 Ω input-output amplifier module. This paper presents the design of the two blocks, discusses issues related to the combining and finally presents the complete amplifier realization and measurement results.**

I. Introduction

Requirements for the RF transmitters used in new wireless communications systems are again tighter. The requirement for the dynamic range of the transmission in GSM system is 28 dB (30 dB in the upper band) whereas in the new WCDMA system it is 65 dB. This together with the modulation method requiring linear transmitter parts forces a new approach to be taken to the transmitter architecture.

The requirement of a larger transmission power control range leads to additional transmitter complexity through a separate gain control circuit. The transmission dynamics in the GSM is typically realized by adjusting the bias of the power amplifier. A similar approach is not applicable in systems that require linear transmitter operation since the bias affects strongly the linearity of the PA. A separate gain control block is needed. It has to be linear enough and provide the whole 65 dB of control range in all operation conditions. The practical realizations typically lead to two separate variable gain amplifiers (VGA) of which one is a separate IC and the other is typically integrated into the transmitter IC containing the other blocks except the PA. Since the whole 65 dB of gain control cannot be realized with only one IC, a variable gain power amplifier seems to be the only choice to reduce the transmitter complexity. In this paper, a power amplifier chip that includes a linear temperature compensated VGA is presented. This approach reduces the transmitter complexity through reducing the number of required ICs. Also the size and cost savings are significant

The amplifier chip is mounted onto a FR-4 type laminate with 26 pcs. of 0402 surface mountable discrete passive components that are used for matching and filtering. The total size of the amplifier module is 8x8x1.8 mm^3. The input is balanced and the output is unbalanced, both matched to 50 Ω. The balun performing the differential-to-single-ended transformation is realized on the laminate with four discrete components.

II. Variable Gain Amplifier Block

The variable gain amplifier block utilizes the classical Gilbert quad topology. The topology is fully differential and the gain control method is current steering. A number of papers have been published by various authors where this same topology has been used successfully [1][2].

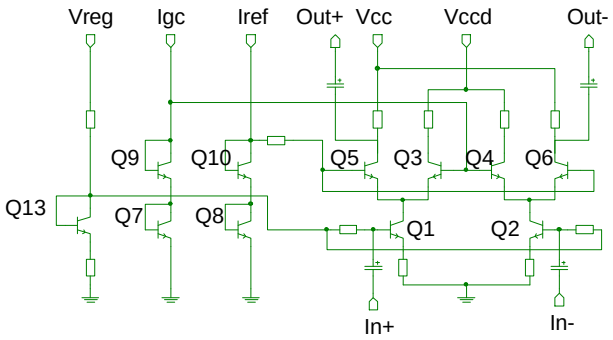

Fig. 1. The schematic of the variable gain amplifier block.

The schematic of the VGA is shown in Fig. 1. *Q1* and *Q2* are the input transistors whose collector current is kept constant with a simple current mirror biasing by *Q13* and a fixed regulated voltage *Vreg*. The common base

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connected transistors *Q5* and *Q6* form the second stage. These together with the current stealing transistors *Q3* and *Q4* form differential pairs whose total collector current is determined by the collector current of the input transistors *Q1* and *Q2*. The two control currents *Igc* and *Iref* determine the balance of the collector currents between the transistors in the differential pairs. The former control current is the actual gain control current and the later is a reference current. The diode connected transistors *Q7, Q8, Q9* and *Q10* form the temperature compensation circuit. The inputs and outputs are DC de-coupled with on-chip capacitors that also take part in the impedance matching. The rest of the input matching of the VGA, which is also the input matching of the whole amplifier, is realized with two surface mountable wire wound inductors on laminate.

An earlier version of the VGA was measured separately in order to define performance bottlenecks. The VGA took 13 mA from a 3.5 V supply voltage and 5 mA from a 2.8 V regulated voltage. The gain control current range is from 10 μA to 4.096 mA and the used reference current was 300 μA.

The linearity of the VGA was excellent. The ACP levels were below -40 dBc over all measurement conditions. The maximum input power to the device was -6 dBm and maximum gain was approximately 3 dB. The VGA achieved approximately 42 dB gain control dynamics in all conditions. The variation of gain was smaller than ±1 dB in temperatures from -25 °C to 85 °C. All the measurements, including the measurements made to the PA block and to the complete amplifier, are made with HPSK modulated signal with peak-to-average ratio of 3.5 dB

The second version of the VGA was designed in order to increase the maximum gain, output power and gain control dynamics. This was accomplished by changing the transistor sizes and load resistors in the collectors of the *Q3, Q4, Q5* and *Q6*. The total gain of the complete variable gain power amplifier increased from 28 dB to 34 dB and the required 24-dBm output power was achieved with -9 dBm input power in all conditions. In the earlier version -6 dBm was needed to reach the output power requirement. Also the gain control dynamics increased slightly. In the earlier version, the dynamics degraded from 42 dB to 38 dB as the VGA was implemented on the same chip with the PA. The minimum achievable attenuation is degraded most likely due to the interference from the PA to the chip ground. In the new version the measured dynamics for the complete variable gain power amplifier is 48 dB so the new VGA by itself should be able to provide more than 50 dB of gain control range.

III. Power Amplifier Block

A push-pull topology is utilized in the PA because the VGA in front of the PA is differential and this way we do not need to convert the input signal from differential to single-ended and therefore the PA can be placed on the same chip easily. Fig. 2 presents the schematic diagram of the chip. All other components presented in this figure are on chip except the inductors labeled *Lbond*. These are used for interstage matching along with discrete chip inductors on the module. The basic concept is almost the same what we used successfully previously in a GSM power amplifier [3]. This time we used only one bias circuit per branch to avoid the possible mismatches in bias currents of the branches that can result from using separate bias circuits. The topology of the output stage bias circuit is such that when temperature increases, it increases the bias current thus compensating the decreasing gain of the AlGaAs/GaAs HBT. The bias circuit of the driver stage is a feedback type bias circuit [5]. It tends to keep the bias current of the driver constant at all temperatures. Therefore the gain of the driver will decrease with increasing temperature. In this design the bias circuit is tuned so that it increases the bias current slightly with temperature compensating the gain degradation. The combined gain performance of the two stages is such that simulations predict less than 1.0 dB gain variation for a temperature range from –25 °C to 85 °C. The driver stage operates very close to class A and the output stage is biased to class AB. Parallel resistors were used between the inputs both at the output stage and the driver. These resistors help in linearizing and also stabilizing the amplifier against possible odd-mode oscillations. Both stages were grounded with viaholes through the chip.

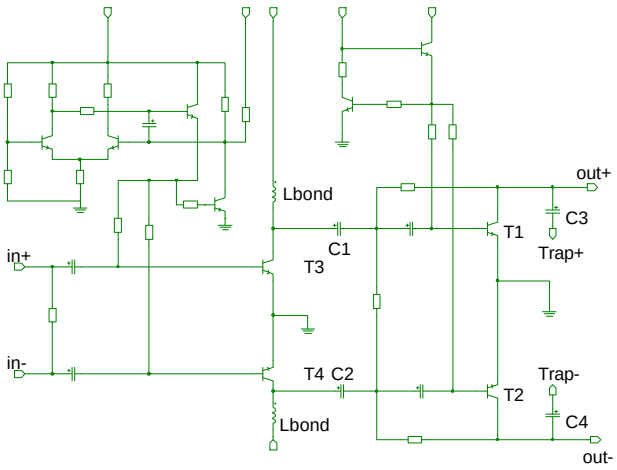

Fig. 2. Schematic diagram of the WCDMA power amplifier

The power amplifier was measured separately on a same FR-4 type module as the whole VGA – PA chip. The operating voltage was kept at 3.5 V for all the measurements. The amplifier was found out to be stable at all operating conditions and also against load mismatches up to VSWR 3:1. Although the power at the output is combined with a lumped element LC – CL balun [4] so that for one branch the response is high-pass and for the other low-pass, the mismatch did not deteriorate the performance of the amplifier considerably. Only small changes could be observed in the measured gain, output power and ACP values.

The efficiency of the PA module with 3.5 V operating voltage was measured to be 36 % when the output power was 24 dBm. At this point the adjacent channel power (ACP1) was -42 dBc and the next adjacent channel power (ACP2) was -55 dBc. With a 3.3 V operating voltage the PA achieved power added efficiency of 38 % and ACP1 = -38 dBc, which still fulfills the linearity specification of ACP1 < -36 dBc.

IV. Complete Variable Gain Power Amplifier

A. Implementation issues

Finally the complete variable gain amplifier was constructed by combining the separately designed VGA and PA blocks on the same chip. Both blocks are differential which makes the combining easier. The chip has 19 input/output pins that are wirebonded to the module. The control currents and voltages are the same as for the individual blocks described in the previous chapters.

The schematic of the VGA – PA module is shown in Fig. 3. The inter-function matching between the VGA block and PA block was realized with on-chip series capacitors and off-chip parallel inductors. Seven capacitors are used only for control and supply voltage bypassing and are not necessarily needed.

B. Measurements

The amplifier operated as predicted in the simulations and did not need any tuning in the laboratory. No oscillations were observed during measurements although the GaAs HBTs and single chip multistage amplifiers tend to be very prone to instability in general.

The amplifier draws 103 mA DC current from the 3.5 V supply and 14 mA from the regulated voltage without an input signal and in a nominal temperature of 25 °C. In addition to the supply and regulated voltages, a reference and a gain control current for the VGA block and a fixed Vpc voltage for the PA are needed.

The measured output power at 1.95 GHz as a function of the control current in different temperatures (-25 to 85 °C) is shown in Fig. 4. The variation of output power in temperatures is less than ±1.8 dB and the shape of the curve is nice and smooth. The required maximum output power 24 dBm is reached in all temperatures.

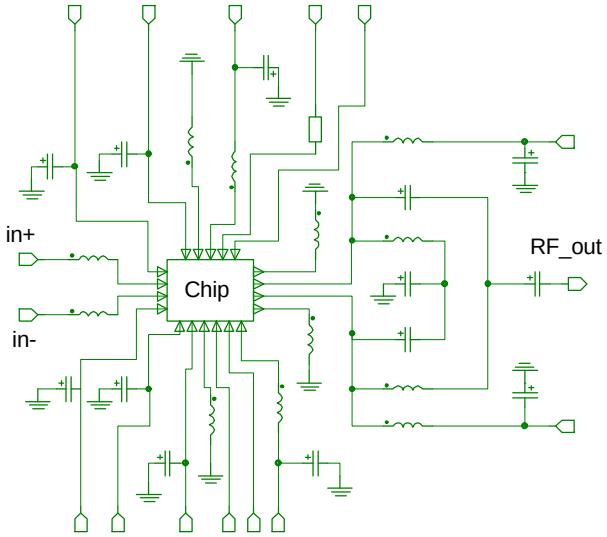

Fig. 3. The schematic of the VGA – PA module.

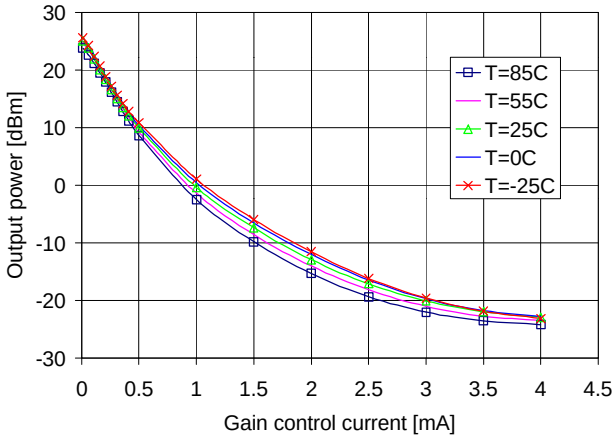

Fig. 4. Measured output power at 1.95 GHz as a function of control current in different temperatures. The input power is kept constant at –9 dBm.

The linearity of the amplifier is good, the ACP figures are below -36 dBc in all the measurement conditions and the output power requirement of 24 dBm is fulfilled. The power added efficiency of the whole amplifier at 24 dBm is > 27 % at minimum and a peak of 39 % was measured at 1.92 GHz center frequency and -25 °C ambient temperature. In that measurement point, the output power

was 26 dBm and the linearity requirements were fulfilled. The nominal performance values with 24-dBm output power are 28 % and ACP1 -41.6 dBc at 1.95 GHz. The adjacent channel leakage power and the power-added efficiency at 1.95 GHz are shown in Fig. 5. The increase in the ACP figures as the output power drops below 0 dBm is due to the measurement setup. The noise floor of the analyzer starts to distort the measurement results at low output power levels.

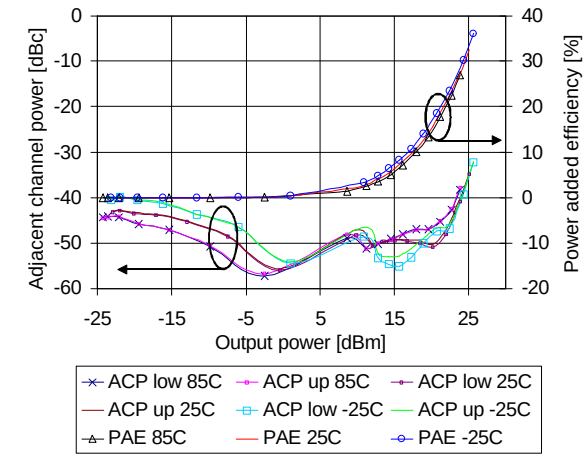

Fig. 5. Measured adjacent channel leakage power and power added efficiency at 1.95GHz as a function of output power. The input power is –9 dBm.

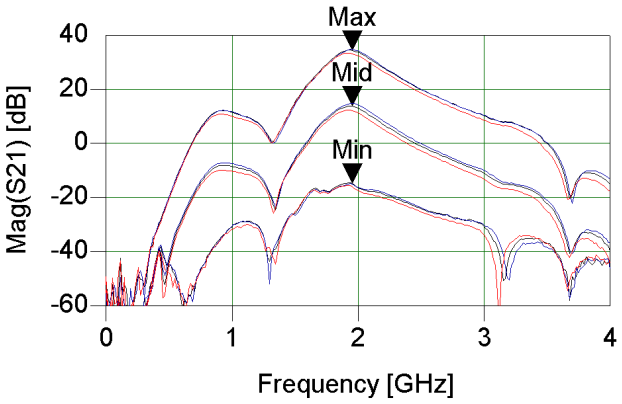

Fig. 6. Measured S_{21} of the amplifier at three different gain control currents (10, 700 and 4096 µA) and in three different temperatures (-25, 25 and 85 °C) as a function of frequency (from 0 to 4 GHz). Measurement power is –20 dBm.

The scattering parameters were measured over the whole temperature range and at three different *Igc* values. The shape of the magnitude curve of the S_{21} is shown in Fig. 6. The small change in temperatures can be viewed in the curve labeled *Mid* that corresponds to the *Igc* = 700 µA. The –10 dB bandwidth of the S_{11} is as wide as 288 MHz in all temperature and *Igc* values whereas the requirement was only 60 MHz (from 1.92 GHz to 1.98 GHz).

V. Conclusions

A linear variable gain power amplifier was realized as a single chip solution. Also accurate temperature compensation was realized with a simple circuitry implemented on the same chip as the amplifier. The amplifier showed a maximum gain variation of ± 1.8 dB over the whole temperature range, an output power 24 dBm with an efficiency greater than 27 %. A peak of 39 % with the output power 26 dBm was measured while fulfilling the required –36 dBc ACP figures. The physical size of the 50 Ω - 50 Ω amplifier module including all the required components is 8x8x1.8 mm^3 (0.115 cc).

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